Application Note: SY6974B

3A, Single Cell Li-Ion DC/DC Switching Charger with I²C Control, USB Detection and OTG JEITA Compliant, Power Path Management

General Description

The SY6974 is a fully-integrated switching battery charger with system power path management devices for single cell Li-ion and Li-polymer battery in a wide range of tablet and other portable devices. Its low impedance power path optimizes switching conversion efficiency, reduces battery charging time and extends battery life during the discharging mode. The I²C serial interface with charging and system settings makes the device a truly flexible solution.

The device supports a wide range of input sources, including standard USB port and high power DC adapter. The SY6974 takes the result from detection circuit in the system, such as USB PHY device. The SY6974 meets USB On-the-Go operation power rating specification by supplying 5.15V (programmable) on BUS with current limit up to 1.2A (programmable).

The power path management regulates the system voltage slightly above battery voltage but does not drop below 3.5V minimum system voltage (programmable). With this feature, the switching converter will keep working to support the system load even when the battery is completely depleted or removed. When the input current limit or voltage limit is reached, the power path management will reduce the charging current to zero firstly. If the system load continues to increase, the power path will discharge the battery to provide the power required by system. This supplement mode operation prevents overloading the input source.

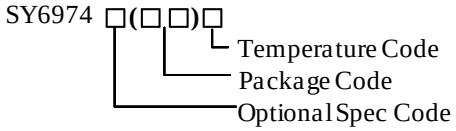
The device initiates and completes a charging cycle without software control. It automatically detects the battery voltage and charges the battery in five phases: battery short, preconditioning, constant current and constant voltage and top-off charging (optional). At the end of the charging cycle, the charger automatically will terminate when the charge current is below a preset limit in the constant voltage phase. When the full battery falls below the recharge threshold, the charger will automatically start another charging cycle. The SY6974 can be compliant with JEITA spec for the 4.2V Li-ion battery.

The device provides various safety features for battery charging and system operation, including negative thermistor monitoring, charging safety timer and over-voltage / over-current protections. The thermal regulation will reduce charge current when the junction temperature exceeds 110℃ (programmable).

The STAT output reports the charging status and any fault conditions. The /PG output in the SY6974 indicates if a good power source is present. The INT immediately will notify the host when a fault occurs.

The SY6974 are available in QFN4x4-24 package.

Ordering Information



Ordering Number	Package type	Note
SY6974QCC	QFN4x4-24	

Features

- High Efficiency 3A 1.5MHz Buck Mode Charger
  - Support 3.9V-13.5V Input Voltage Range
  - Programmable IDPM/VDPM to Support the USB and Adapter
  - 3.856V-4.624V Adjustable Charge Voltage
  - Support Narrow VDC Power Path Management
  - JEITA Compliance
  - ±0.5% Charge Voltage Regulation
  - Charge Status Outputs for LED or Host Processor
- Maximum 1.2A 1.5MHz Boost OTG Current
  - 4.85V-5.3V Adjustable OTG Output Voltage
  - Selectable OTG Output Current Limit
  - ± 1.5% Output Regulation in Boost Mode
  - Soft-Start up to 500 µF Capacitive Load
  - Constant Current (CC) Limit
- Full BATFET Control to Support Shipping Mode, Wake up, and System Reset
- Safety
  - Battery Temperature Sensing for Charge and Boost Mode
  - Battery Charging Safety Timer
  - Thermal Regulation and Thermal Shutdown
  - Input/System over-Voltage Protection
  - MOSFET over-Current Protection
- Low Battery Leakage Current and Support Shipping Mode
- 4mm x 4mm QFN-24 Package

Applications

- Smart Phone
- Tablet PC
- Power Bank
- Portable Internet Devices

Typical Application

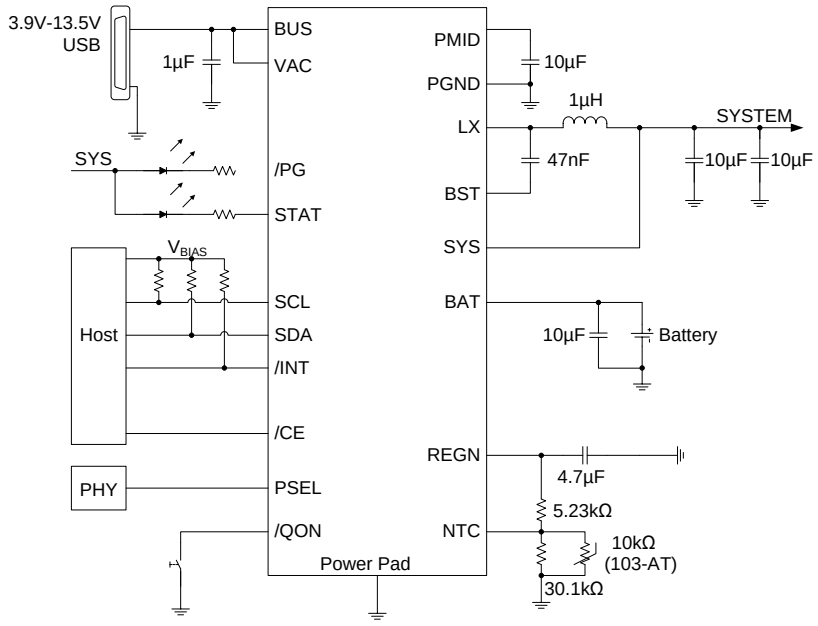
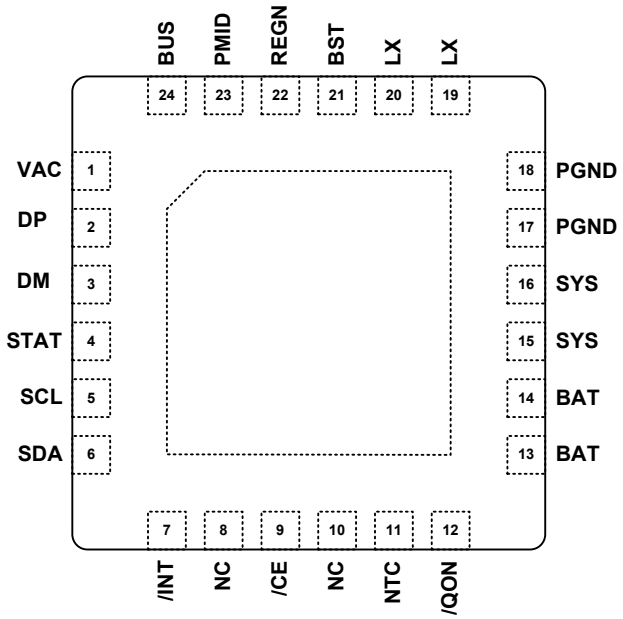


Figure 1. Schematic Diagram

Pinout



(QFN4x4-24)

Top Mark: CUE*xyz*(device code: **CUE**, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin No	Pin Description
VAC	1	Charge input voltage sense. This pin must be connected close to BUS pin.
PSEL	2	Power source selection input. High indicates a USB host source and Low indicates an adapter source. In default mode, set 500mA input current limit by pulling this pin high and set 2.4A input current limit by pulling this pin low.
/PG	3	Open drain active low power good indicator. Connect to the pull up rail via 10kΩ resistor. Low indicates a good input source.
STAT	4	Open drain charge status output to indicate various charger operation. Connect to the pull up rail via 10kΩ resistor. Low indicates charge in progress. High indicates charge complete or charge disabled. When any charge fault condition occurs, STAT pin will blink at 1Hz. The STAT pin function can be disabled when STAT_DIS bit is set.
SCL	5	I^2C Interface clock. Connect SCL to the logic rail through a 10kΩ resistor.
SDA	6	I^2C Interface data. Connect SDA to the logic rail through a 10kΩ resistor.
/INT	7	Open-drain interrupt output. Connect the /INT to a logic rail via 10kΩ resistor. The /INT pin sends active low, 256μs pulse to host to report charger device status and fault.
NC	8, 10	No connect.
/CE	9	Active low charge enable pin. Battery charging will be enabled when REG01[4]=1 and /CE pin =Low. /CE pin must be pulled high or low.
NTC	11	Connect a resistor divider from REGN to NTC to GND to achieve battery thermal protection. Charge will suspend when NTC pin is out of range. Recommend 103AT-2 thermistor.

/QON	12	BATFET enable control in shipping mode and BATFET reset function. When BATFET is in shipping mode, logic high to low transition on this pin with minimum of T_{QON_LOW} low level will turn on BATFET to exit shipping mode. This pin is internally pulled up to default high logic. When BUS is not plugged in and BATFET_DIS=0, a logic low of T_{QON_RST} will reset SYS (system power) by turning BATFET off for T_{BATFET_RST} and then re-enable BATFET.
BAT	13,14	Battery connection point to the positive terminal of the battery pack. The internal BATFET is connected between BAT and SYS. Connect a 10μF closely to the BAT pin
SYS	15,16	System connection point. The internal BATFET is connected between BAT and SYS. When the battery falls below the minimum system voltages, switch mode converter will keep SYS above the minimum system voltage.
PGND	17,18	Power ground connection node. Internally, PGND is connected to the source of the n-channel LSFET. On PCB layout, connect directly to ground connection of input and output capacitors of the charger.
LX	19,20	Switching node pin. Connect to external inductor.
BST	21	HSFET driver positive supply. Connect a 47nF bootstrap capacitor from LX to BST.
REGN	22	LSFET driver positive supply. Connect a 4.7μF ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN also serves as bias rail of NTC pin.
PMID	23	Connected to the drain of the reverse blocking MOSFET and the drain of HSFET. Put at least 10μF on PMID to PGND, and place it as close as possible to IC.
BUS	24	Charger power input pin. Place a 1μF ceramic capacitor from BUS to PGND and place it as close as possible to IC.
Exposed pad	-	Exposed pad beneath the IC for heat dissipation. Always solder exposed pad to the board, and have vias on the Power Pad plane star-connecting to PGND and ground plane for high current power converter.

Absolute Maximum Ratings (Note 1)

BUS, VAC, PMID, LX ---------- -0.3V to +18V
BAT, SYS, REGN, PSEL, /PG, STAT, SCL, SDA, /INT, /CE, NTC, /QON, BST-LX ---------- -0.3V to +6V
Package Thermal Resistance (Notes 2)

θ_{JA} ----------
θ_{JC} (top) ----------
θ_{JB} ----------
ψ_{JT} ---------- 0.35℃/W

Junction Temperature Range ---------- -40℃ to +150℃
Operating Temperature Range ---------- -40℃ to +150℃
Storage Temperature ---------- -65℃ to +150℃
Lead Temperature (Soldering, 10s) ---------- +300℃

ESD Susceptibility
HBM (Human Body Mode) ---------- 2kV
CDM (Charged Device Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

BUS, VAC, PMID, LX ---------- 0V to +16V
BAT, SYS, REGN, PSEL, /PG, STAT, SCL, SDA, /INT, /CE, NTC, /QON, BST-LX ---------- 0V to +5.5V
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃

Block Diagram

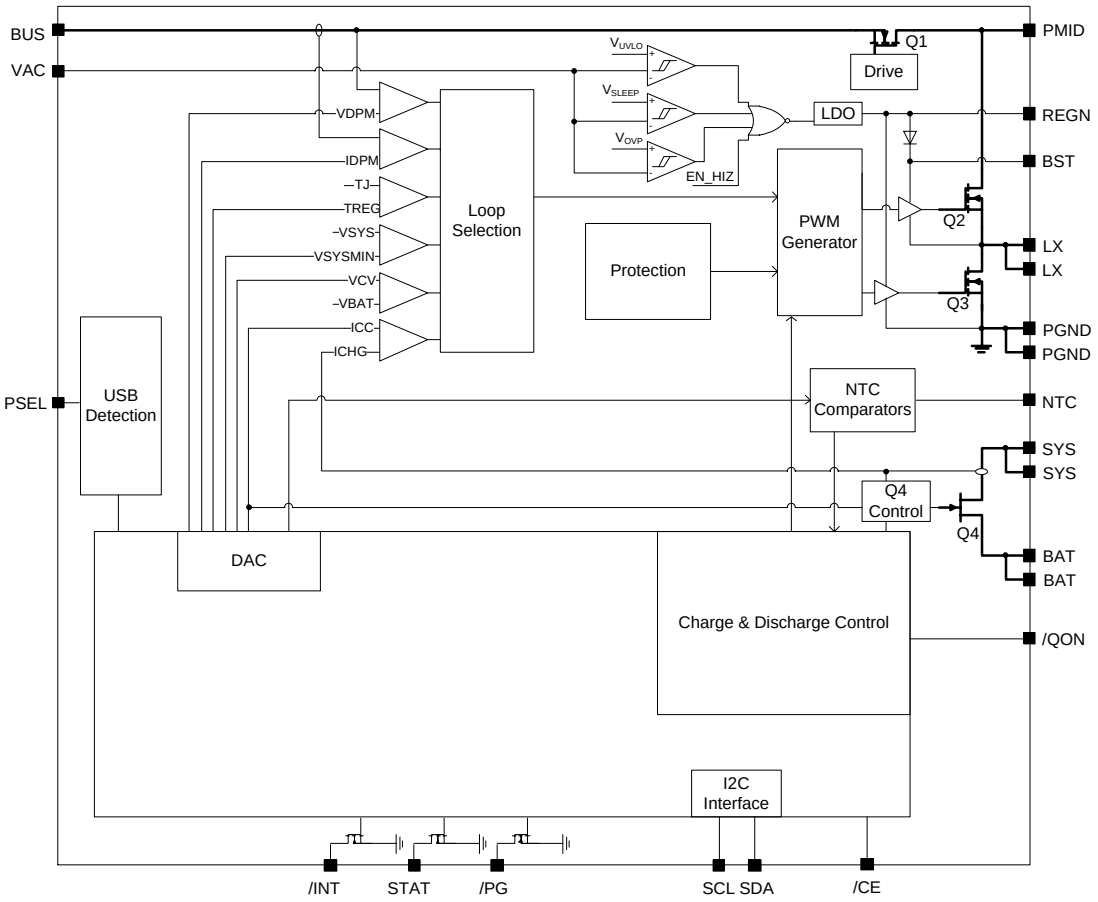


Figure 2. Block Diagram

Electrical Characteristics

(V_{BUS_UVLOZ}<V_{BUS}<V_{ACOV} and V_{BUS}>V_{BAT}+V_{SLEEPZ}, T_J=25℃ for typical values unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Currents						
Battery Discharge Current (BAT)	DP DM I_{BAT}	V_{BUS}<V_{BUS_UVLOZ}, V_{BAT}=4.5 V, leakage between BAT and BUS			5	μA
		V_{BAT}=4.5 V, High-Z Mode, no BUS, BATFET disabled		15	25	μA
		V_{BAT}=4.5 V, High-Z Mode, no BUS, BATFET enabled		40	55	μA
Input Supply Current in High-Z Mode	I_{BUS_HIZ}	V_{BUS}=5V, no battery, High-Z mode enabled		20	35	μA
		V_{BUS}=12V, no battery, High-Z mode enabled		25	50	μA
Input Supply Current (BUS)	I_{BUS}	V_{BUS}>V_{BUS_UVLOZ}, V_{BUS}>V_{BAT}, converter not switching		1.5	3	mA
		V_{BUS}> V_{BUS_UVLOZ}, V_{BUS}>V_{BAT}, converter switching, V_{BAT}=3.8V, I_{SYS}=0A		3		mA
Battery Discharge Current in Boost Mode	$I_{OTGBOOST}$	V_{BAT}=4.2V, Boost mode, I_{BUS}=0A, converter switching		3.5		mA
BUS/BAT Power up						
BUS Operating Range	V_{BUS_OP}		3.9		13.5	V
BUS for Active IC and I²C, no Battery	V_{BUS_UVLOZ}	Rising value to active I²C		3.3	3.5	V
		Falling value		2.9	3.25	V
Sleep Mode Falling Threshold	V_{SLEEP}	V_{BUS} falling, V_{BUS}-V_{BAT}	25	65	120	mV
Sleep Mode Rising Threshold	V_{SLEEPZ}	V_{BUS} rising, V_{BUS}-V_{BAT}	170	250	300	mV
BUS over-Voltage Rising Threshold	V_{ACOV}	V_{BUS} rising, REG06[7:6]=00	5.7	5.9	6.1	V
BUS over-Voltage Recovery Threshold	V_{ACOV_RC}	V_{BUS} falling, REG06[7:6]=00	5.5	5.7	5.9	V
BUS over-Voltage Rising Threshold	V_{ACOV}	V_{BUS} rising, REG06[7:6]=11	13.8	14.1	14.4	V
BUS over-Voltage Recovery Threshold	V_{ACOV_RC}	V_{BUS} falling, REG06[7:6]=11	13.5	13.8	14.1	V
Battery for Active I²C, no BUS	V_{BAT_UVLOZ}	V_{BAT} rising value to active I²C		2.1	2.3	V
		V_{BAT} falling		1.8	2.0	V
Battery Depletion Threshold	V_{BAT_DPL}	V_{BAT} falling	2.15	2.3	2.5	V
Battery Depletion Recovery Threshold	V_{BAT_DPLZ}	V_{BAT} rising	2.3	2.55	2.7	V
Bad Adapter Detection Threshold	V_{BUSMIN}	V_{BUS} falling	3.6	3.7	3.8	V
Bad Adapter Detection Hysteresis	V_{BUSMIN_HYST}	V_{BUS} rising		100		mV
Bad Adapter Detection Current Source	I_{BADSRC}			30		mA
Bad Source Detection Duration	t_{BADSRC}			30		ms
Power Path Management						
System Regulation Voltage	V_{SYS_MAX}	I_{SYS} = 0A, V_{BAT}>V_{SYSMIN}, BATFET off, V_{BAT} up to 4.35V, V_{SYS}=V_{BAT}+50mV	4.35	4.4	4.43	V
System Regulation Voltage	V_{SYS_MIN}	I_{SYS}=0A, V_{BAT}<V_{SYSMIN}=3.5V,	3.55	3.65	3.75	V

		BATFET off, $V_{SYS}=V_{BAT}+150mV$				
Internal High-side Reverse Blocking MOSFET on Resistance	$R_{ON(RBFET)}$			45		mΩ
Internal High-side Switching MOSFET on Resistance between PMID and LX	$R_{ON(HSFET)}$			60		mΩ
Internal low-side Switching MOSFET on Resistance between LX and PGND	$R_{ON(LSFET)}$			60		mΩ
BATFET Forward Voltage in Supplement Mode	V_{FWD}	BAT discharge current 10mA		30		mV
Battery Charger						
Charge Voltage Regulation Accuracy	$V_{BAT\_REG\_ACC}$	V_{BAT_REG} = 4.208V and 4.352V	-0.5%		0.5%	
Fast Charge Current Regulation Accuracy	$I_{ICHG\_REG\_ACC}$	V_{BAT}=3.8V, I_{CHG}=0.72A or 1.38A	-5.5%		5.5%	
Battery LOWV Falling Threshold	$V_{BATLOWV}$	Fast charge to precharge, VBAT falling	2.6	2.8	2.9	V
Battery LOWV Rising Threshold	$V_{BATLOWV\_HYST}$	Precharge to fast charge, VBAT rising	2.8	3.0	3.1	V
Precharge Current Regulation Accuracy	I_{PRECHG_ACC}	V_{BAT} = 2.6V, I_{CHG} = 180mA	-15%		20%	
Termination Current Accuracy	I_{TERM_ACC}	I_{TERM} =180mA, I_{CHG_REG} >780mA	-20%		20%	
		I_{TERM} =60mA, I_{CHG_REG} ≤780mA	-35%		35%	
Battery Short Voltage	V_{SHORT}	V_{BAT} falling	1.9	2.0	2.1	V
Battery Short Voltage Hysteresis	V_{SHORT_HYST}	V_{BAT} rising		200		mV
Battery Short Current	I_{SHORT}	V_{BAT}<2.2V	55	100	125	mA
Recharge Threshold Below V_{BAT_REG}	V_{RECHG}	V_{BAT} falling, REG04[0] = 0	75	100	145	mV
		V_{BAT} falling, REG04[0] = 1	160	200	250	mV
SYS-BAT MOSFET on Resistance	R_{ON_BATFET}			17		mΩ
Input Voltage/Current Regulation						
Absolute Input Voltage Regulation Accuracy	$V_{INDPM\_REG\_ACC}$	set absolute VINDPM=4.5V	-1.5%		1.5%	
Input Current Limit Range	I_{INDPM_RANGE}		100		3200	mA
USB Input Current Regulation Limit, BUS=5V, Current Drawn from LX	I_{USB_DPM}	USB 100mA	80		100	mA
		USB 500mA	440		500	
		USB 900mA	750		900	
Input Current Regulation Accuracy	I_{ADPT_DPM}	I^2C Set input current limit above 900mA	-15%	-7%	0%	
BAT over-Voltage Protection						
Battery over-Voltage Threshold	V_{BATOVP}	V_{BAT} rising, as percentage of V_{BAT_REG}	103%	104%	105%	
Battery over-Voltage Hysteresis	V_{BATOVP_HYST}	V_{BAT} falling, as percentage of V_{BAT_REG}		2%		
BAT Discharge over-Current Protection						
BATFET Discharge over-Current Threshold	I_{BATFET_OCP}		7.5	10	12.5	A
Thermal Regulation and Thermal Shutdown						
Junction Temperature Regulation Accuracy	$T_{Junction\_REG}$	REG05[1]=1		110		℃
Thermal Shutdown Rising Temperature	T_{TSD}	Temperature increasing		160		℃

Thermal Shutdown Hysteresis	T_{TSD_HYS}			30		℃
JEITA Thermister Comparator						
T1(0 ℃) Threshold, Charge Suspended Below this Temp	V_{T1}	V_{NTC} rising, as percentage to V_{REGN}, JEITA_ISET=0	72.75	73.25	73.75	%
Charge back to I_{CHG}/2 and V_{REG} above this Temp	V_{T1_HYS}	Hysteresis, V_{NTC} falling, JEITA_ISET=0		1.25		%
T2(10 ℃) Threshold, Charge back to I_{CHG}/2 and V_{REG} below this Temp	V_{T2}	V_{NTC} rising, as percentage to V_{REGN}, JEITA_ISET=0	67.75	68.25	68.75	%
Charge back to I_{CHG} and V_{REG} above this Temp	V_{T2_HYS}	Hysteresis, V_{NTC} falling, JEITA_ISET=0		1.25		%
T3(45 ℃) Threshold, Charge back to I_{CHG} and 4.05V above this Temp	V_{T3}	V_{NTC} falling, as percentage to V_{REGN}, JEITA_VSET=0	44.25	44.75	45.25	%
Charge back to I_{CHG} and V_{REG} below this Temp	V_{T3_HYS}	Hysteresis, V_{NTC} rising, JEITA_VSET=0		1.2		%
T4(60 ℃) Threshold, Charge Suspended above this Temp	V_{T4}	V_{NTC} falling, as percentage to V_{REGN}, JEITA_VSET=0	33.7	34.2	34.7	%
Charge back to I_{CHG} and 4.05V below this Temp	V_{T4_HYS}	Hysteresis, V_{NTC} rising, JEITA_VSET=0		1.2		%
Boost Mode Thermister Comparator						
Cold Temperature (-20 ℃) Threshold 1, NTC pin Voltage Rising Threshold	V_{BCOLD}	As Percentage to V_{REGN}	79.5	80	80.5	%
Falling Hysteresis	V_{BCOLD_HYS}			1.25		%
Hot Temperature (65 ℃) Threshold 2, NTC pin Voltage Falling Threshold	V_{BHOT}	As Percentage to V_{REGN}	30.6	31.1	31.6	%
Rising Hysteresis	V_{BHOT_HYS}			3		%
Buck Mode Operations						
HSFET Cycle-by-cycle Current Limit	I_{HSFET_OCP}			6		A
PWM Switching Frequency	F_{SW}		1300	1500	1700	kHz
Boost Mode Operations						
PWM Switching Frequency	F_{SW_BOOST}	V_{BAT}=3.2V, V_{BUS}=5V, I_{BUS}=1A	1300	1500	1700	kHz
OTG Output Voltage Range	V_{OTG_REG}	I_{BUS}=0A	4.85		5.3	V
OTG Output Voltage Accuracy	$V_{OTG\_REG\_ACC}$	I_{BUS}=0A	-1.5%		1.5%	
Battery Voltage Exiting Boost Mode	V_{OTG_BAT}	REG01[0]) = 0, V_{BAT} falling	2.6	2.8	2.9	V
Battery Voltage Entering Boost Mode	$V_{OTG\_BAT\_HYST}$	REG01[0]) = 0, V_{BAT} rising	2.7	2.9	3.0	V
Battery Voltage Exiting Boost Mode	V_{OTG_BAT}	REG01[0]) = 1, V_{BAT} falling	2.4	2.5	2.6	V
Battery Voltage Entering Boost Mode	$V_{OTG\_BAT\_HYST}$	REG01[0]) = 1, V_{BAT} rising	2.55	2.65	2.75	V
OTG Mode Output Constant Current Limit	I_{OTG}	BOOST_LIM=0.5A	0.55		0.75	A
		BOOST_LIM=1.2A	1.25		1.65	A
OTG over-Voltage Threshold	V_{OTG_OVP}	BUS rising edge	5.7	5.85	6	V
OTG over-Voltage Threshold Hysteresis	$V_{OTG\_OVP\_HYS}$	BUS falling edge		250		mV
REGN LDO						
REGN LDO Output Voltage	V_{REGN}	V_{BUS} = 10V, I_{REGN} = 40mA		5		V
		V_{BUS} = 5V, I_{REGN} = 20mA		4.8		V

REGN LDO Current Limit	I_{REGN}	V_{BUS} = 5V, V_{REGN} = 3.8V	50			mA
/QON Timing						
/QON Low Time to Turn on BATFET and Exit Ship Mode	T_{QON_LOW}		0.9	1.1	1.3	s
/QON Low Time to Reset BATFET	T_{QON_RST}		8	10	12	s
Reset Duration(BATFET off Time)	T_{BATFET_RST}		0.25	0.35	0.45	s
Enter Ship Mode Delay	t_{SM_DLY}	BATFET_DIS=1, BATFET_DLY=1	10	13	15	s
Logic I/O Pin Characteristics (/CE, PSEL, STAT, /PG, /INT)						
Input Low Threshold	V_{ILOW}				0.4	V
Input High Threshold	V_{IHGH}		1.3			V
Output Low Saturation Voltage	V_{OUT_LOW}				0.4	V
Internal /QON Pull up	R_{QON}			220		kΩ
I^2C Interface (SDA, SCL)						
Input High Threshold Level	V_{IH}		1.3			V
Input Low Threshold Level	V_{IL}				0.4	V
Output Low Threshold Level	V_{OL}				0.4	V
SCL Clock Frequency	f_{SCL}				400	kHz
Digital Clock and Watchdog Timer						
Watchdog Timeout	t_{WDT}	REGN LDO disabled, REG05[5:4]=11	112	160	208	s
		REGN LDO enabled, REG05[5:4]=11	136	160	184	s

Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

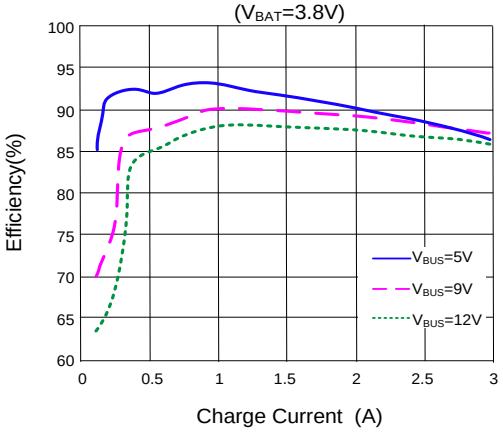
Note 2: θ_{JA} is tested under still air while ambient temperature 25℃ and mounted on a 4-layer high effective PCB with thermal via in accordance with JESD51-5, -7.

Note 3: The device is not guaranteed to function outside its operating conditions.

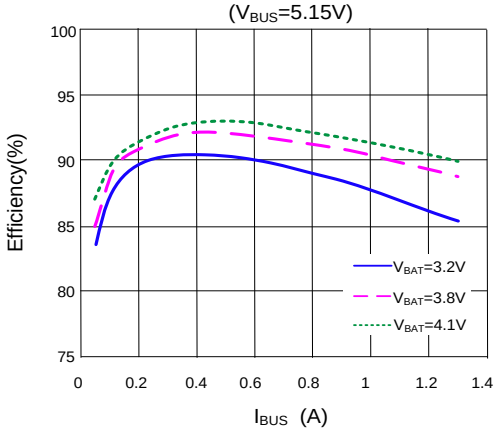
Typical Performance Characteristics

T_A=25℃, V_{BUS}=5V, 1cell battery, unless otherwise specified.

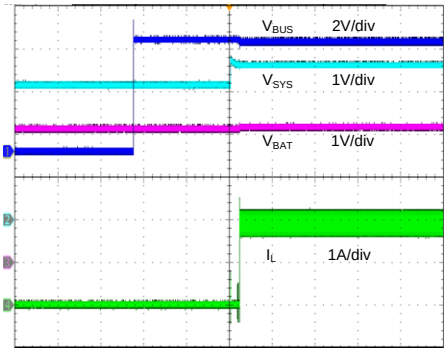
Efficiency vs. Charge Current (CC Mode)
(V_{BAT}=3.8V)



Efficiency vs. I_{BUS} (Boost Mode)
(V_{BUS}=5.15V)

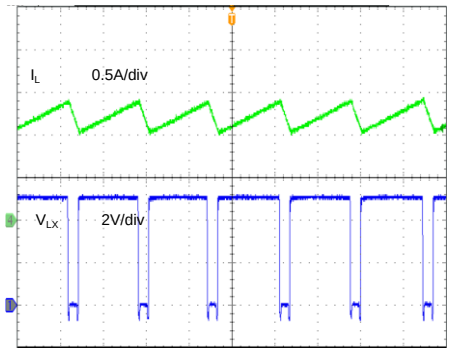


Adapter Plug-in in Default Mode
(V_{BAT}=3.1V)



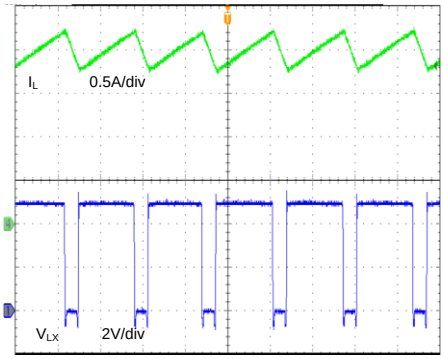
Time (100ms/div)

CV Mode Steady State
(V_{BAT}=4.2V)



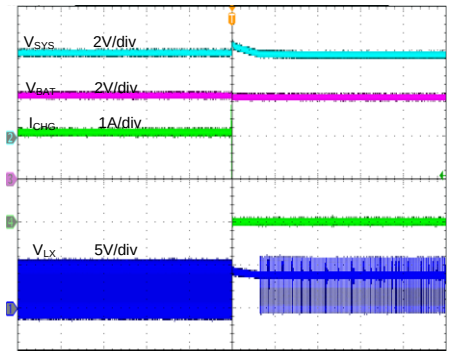
Time (400ns/div)

CV Mode Steady State
(V_{BAT}=3.7V)



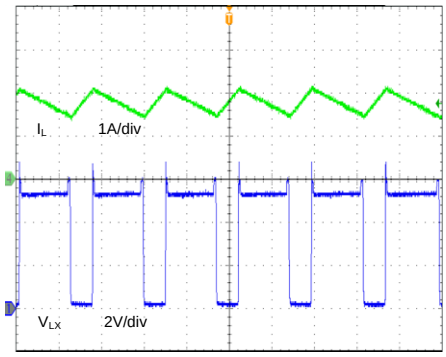
Time (400ns/div)

Charge Enable to Disable
(I_{SYS}=15mA)



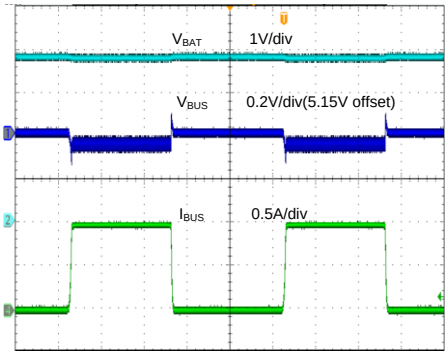
Time (800µs/div)

Boost Mode Steady State
(I_{SYS}=1.2A)



Time (1μs/div)

Boost Mode Load Transient



Time (4ms/div)

I²C Registers

Address: 6BH

REG00

BIT	Name	POR	Description
7	EN_HIZ	0	**Enable HIZ Mode:** 0–Disable (Default); 1–Enable
6:5	STAT_DIS[1:0]	00	**Enable STAT pin function:** 00 - Enable STAT pin function(Default) 01 – Reserved 10 – Reserved 11 - Disable STAT pin function(float)
4:0	IINLIM[4:0]	00100	**Input current limit:** (Actual input current limit by PSEL detection in default mode, and by this register in host mode) IINLIM=100mA+100mA*[IINLIM] Range:100mA(00000)-3.2A(11111) 00000=100mA 00001=200mA … 00100=500mA(Default) … 11111=3.2A IINLIM will be changed after input detection is completed. (PSEL=High) 500mA (PSEL=Low) 2.4A Host can over-write IINDPM register bits after input source detection is completed.

REG01

BIT	Name	POR	Description
7	PFM _DIS	0	**PFM mode Disable**: 0- Enable PFM(Default) 1- Disable PFM
6	WD_RST	0	**I²C Watchdog Timer Reset:** 0-Normal(Default) 1-Reset Back to 0 after watchdog timer reset.
5	OTG_CONFIG	0	**OTG Mode Configuration:** 0-OTG Disable(Default) 1-OTG Enable Note: OTG_CONFIG would over-ride Charge Enable Function in CHG-CONFIG
4	CHG_CONFIG	1	**Charge Enable Configuration:** 0-Charge Disable 1-Charge Enable(Default)

3:1	SYS_MIN[2:0]	101	**Minimum System Voltage Limit:** Range:2.6V-3.7V 000=2.6V 001=2.8V 010=3.0V 011=3.2V 100=3.4V 101=3.5V(Default) 110=3.6V 111=3.7V
0	OTG_BAT	0	0 – 2.8 V BAT falling(Default) 1 – 2.5 V BAT falling

REG02

BIT	Name	POR	Description
7	BOOST_LIM	1	**Boost Mode Current minimum Limit:** 0 = 0.5 A 1 = 1.2 A(Default)
6	Q1_FULLON	0	**RBFET full on for better efficiency in Buck mode:** 0 – Use higher Q1 $R_{DS(ON)}$ when programmed IINDPM ≤ 700mA(better accuracy) 1 – Use lower Q1 $R_{DS(ON)}$ always(better efficiency)
5:0	ICHG[5:0]	100010	**Fast Charge Current Limit:** ICHG=[ICHG]*60mA Range:0mA(000000)-3000mA(110010) 000000=0mA(Disable Charge) 000001=60mA … 100010=2040mA(Default) … 110010~111111=3000mA

REG03

BIT	Name	POR	Description
7:4	IPRECHG [3:0]	0010	**Precharge Current Limit:** IPRECHG=60mA+[IPRECHG]*60mA Range:60mA-780mA 0000=60mA … 0010=180mA(Default) … 1100~1111=780mA
3:0	ITERM [3:0]	0010	**Termination Current Limit:** ITERM=60mA+[ITERM]*60mA Range:60mA-960mA 0000=60mA … 0010=180mA(Default)

			… 1100=780mA … 1111=960mA

REG04

BIT	Name	POR	Description
7:3	VREG[4:0]	01011	**Charge Voltage Limit:** VREG=3.856V+[VREG]*32mV Range:3.856V-4.624V(11000) 00000=3.856V 00001=3.888V … 01011=4.208V(Default) … 11000~11111=4.624V Special Value: (01111): 4.352 V
2:1	TOPOFF_TIMER[1:0]	00	**The extended charging time after termination enabled and satisfied:** 00 – Disabled (Default) 01 – 15 minutes 10 – 30 minutes 11 – 45 minutes
0	VRECHG	0	**Battery Recharge Threshold Offset:** 0-100mV(Default) 1-200mV

REG05

BIT	Name	POR	Description
7	EN_TERM	1	**Charging Termination Enable:** 0-Disable 1-Enable(Default)
6	Reserved	0	Reserved
5:4	WATCHDOG[1:0]	01	**I²C Watchdog Timer Setting:** 00-Disable timer 01-40s(Default) 10-80s 11-160s
3	EN_TIMER	1	**Charging Safety Timer Enable:** 0-Disable 1-Enable(Default)
2	CHG_TIMER	1	**Fast Charge Timer Setting:** 0-5 hrs 1-10 hrs(Default)
1	TREG	1	**Thermal Regulation Threshold:** 0-90℃ 1-110℃(Default)

0	JEITA_ISET (0℃-10℃)	1	**JEITA Low Temperature Current Setting** Percentage with respect to ICHG register REG02[5:0] 0-50% 1-20%(Default)

REG06

BIT	Name	POR	Description
7:6	OVP[1:0]	01	**ACOV threshold:** 00 - 5.5 V 01 – 6.5 V (5-V input) (Default) 10 – 10.5 V (9-V input) 11 – 14 V (12-V input)
5:4	BOOSTV[1:0]	10	**Boost Regulation Voltage:** BOOSTV=4.85V+[BOOSTV]*0.15V Range: 4.85V-5.3V 00=4.85V 01=5.00V 10=5.15V(Default) 11=5.30V
3:0	VINDPM[3:0]	0110	**Absolute VINDPM Threshold:** VINDPM=3.9V+[VINDPM]*100mV Range:3.9V(0000)-5.4V(1111) 0000=3.9V 0001=4.0V … 0110=4.5V(Default) … 1111=5.4V

REG07

BIT	Name	POR	Description
7	FORCE_INDET	0	**Force Start Input Current Limit:** 0-Do not force(Default) 1-Force Returns to 0 after input detection is complete.
6	TMR2X_EN	1	**Safety Timer Setting during Input DPM and Thermal Regulation and JEITA cool:** 0-Safety timer not slowed by 2X during input DPM or thermal regulation or JEITA cool. 1-Safety timer slowed by 2X during input DPM or thermal regulation or JEITA cool. (Default)
5	BATFET_DIS	0	**Force BATFET Off:** 0-Allow Q4 turn on(Default) 1-Turn off Q4 with t_{SM_DLY} delay time or immediately (REG07[3]
4	JEITA_VSET (45℃-60℃)	0	**JEITA High Temperature Voltage Setting:** 0-VREG 4.05V (max.) (Default) 1-VREG

	BATFET_DLY	1	**BATFET turn off delay control:** 0-Turn off BATFET immediately when BATFET_DIS is set. 1-Turn off BATFET with the delay t_{SM_DLY} when BATFET_DIS is set. (Default)
2	BATFET_RST_EN	1	**BATFET Reset Enable:** 0-Disable BATFET reset function 1-Enable BATFET reset function(Default)
1:0	VDPM_BAT_TRACK[1:0]	00	**Limit VINDPM to above BAT voltage.** 00 - Disable function (VINDPM set by register) (Default) 01 - VBAT + 200mV 10 - VBAT + 250mV 11 - VBAT + 300mV When this bit enabled, Actual VINDPM is higher of register value and VBAT + VDPM_BAT_TRACK

REG08 (Read only)

BIT	Name	POR	Description
7:5	BUS_STAT[2:0]	NA	**BUS Status register:** 000:No input 001:USB Host SDP 011:Adapter(2.4A) 111:OTG Note: Software current limit is reported in IINLIM register.
4:3	CHRG_STAT[1:0]	NA	00-Not Charging 01-Pre-charge ($V_{BAT}<V_{BATLOWV}$) 10-Fast Charging 11-Charge Termination Done
2	PG_STAT	NA	**Power Good Status:** 0-Not Power Good 1-Power Good
1	THERM_STAT	NA	**Thermal Regulation Status:** 0-Not in thermal regulation 1- In thermal regulation
0	VSYS_STAT	NA	**VSYS Regulation Status:** 0-Not in SYSMIN regulation ($V_{BAT}>V_{SYSMIN}$) 1-In SYSMIN regulation ($V_{BAT}<V_{SYSMIN}$)

REG09 (Read only)

BIT	Name	POR	Description
7	WATCHDOG_FAULT	NA	**Watchdog Fault status:** 0-Normal 1-Watchdog timer expiration
6	BOOST_FAULT	NA	**Boost Mode Fault Status:** 0-Normal 1-BUS overloaded in OTG, or BUS OVP, or battery is too low

5:4	CHRG_FAULT[1:0]	NA	**Charge Mode Fault Status:** 00-Normal 01-Input fault (BUS OVP or V_{BAT}<V_{BUS}<3.8V) 10-Thermal shutdown 11-Charge Safety Timer Expiration
3	BAT_FAULT	NA	**Battery Fault Status:** 0-Normal 1-BATOVP
2:0	NTC_FAULT[2:0]	NA	**NTC Fault Status:** Buck Mode: 000-Normal 010-NTC Warm 011-NTC Cool 101-NTC Cold 110-NTC Hot Boost Mode: 000-NTC Normal 101-NTC Cold 110-NTC Hot

REG0A

BIT	Name	POR	Description
7	BUS_GD	NA	**BUS GOOD Status:** 0-No BUS attached 1-BUS attached
6	VDPM_STAT	NA	**VINDPM Status:** 0-Not in VINDPM 1-In VINDPM
5	IDPM_STAT	NA	**IINDPM Status:** 0-Not in IINDPM 1-In IINDPM
4	Reserved	NA	
3	TOPOFF_ACTIVE	NA	**Top-off Timer Status:** 0 – Top off timer not counting. 1 – Top off timer counting
2	ACOV_STAT	NA	**BUSOVP Status In Buck Mode:** 0-Normal 1-ACOV
1	VINDPM_INT_MASK	0	**Mask INT when VINDPM:** 0 - Allow VINDPM INT pulse 1 - Mask VINDPM INT pulse
0	IINDPM_INT_MASK	0	**Mask INT when IINDPM:** 0 - Allow IINDPM INT pulse 1 - Mask IINDPM INT pulse

BIT	Name	POR	Description
7	REG_RST	0	**Register Reset:** 0-Keep current register setting(Default) 1-Reset to default register value and reset safety timer Reset to 0 after register reset is completed
6:3	PN[3:0]	NA	**Device Configuration:** 1001
2	Reserved	0	Reserved
1:0	DEV_REV[1:0]	NA	00

Operation Principle

The SY6974 is a fully-integrated switching battery charger with system power path management devices for single cell Li-ion and Li-polymer battery in a wide range of tablet and other portable devices. It integrates the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and BATFET (Q4) between system and battery. The extremely low R_{DSON} achieves very high conversion efficiency up to 3A charging current. The device also integrates the bootstrap diode for the high-side gate drive.

Power on Reset (POR)

The internal bias circuits are powered from the higher voltage between BUS and BAT. When BUS rises above V_{BUS_UVLOZ} or BAT rises above V_{BAT_UVLOZ}, the sleep comparator, battery depletion comparator and BATFET driver will be active. I^2C interface is ready for communication. The host can access all the registers after POR.

Power up from Battery without DC Source

If only battery is present and the voltage is above depletion threshold (V_{BAT_DPLZ}), the BATFET will turn on and provide power to system. The device is in HIZ mode and the REGN LDO stays off to minimize the quiescent current. The low R_{DSON} in BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time. The device always monitors the discharge current through BATFET. When the system is overloaded or shorted, the device will immediately turn off BATFET and latch off and set BATFET_DIS bit to indicate BATFET is disabled until the input source plugs in again or one of the methods describe in section “BATFET Enable Mode” to re-enable BATFET.

Power up from DC Source

When the DC source plugs in, the SY6974 will check the input source voltage to turn on REGN LDO and all the bias circuits. It will also check and set the input current limit before starts the Buck converter.

REGN LDO

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The LDO also provides bias rail to NTC external resistors. The pull-up rail of STAT and /PG can be connected to REGN as well.

When the device is in high impedance mode (HIZ) with REGN LDO turned off, the device will draw less than I_{BUS_HIZ} from BUS during HIZ state. The battery will power up the system when the device is in HIZ mode.

Blocking FET (Q1)

After REGN LDO powers up, the SY6974 will turn on the blocking FET to reduce the power loss.

Input Source Qualification

After REGN LDO power up, the SY6974 will check the current capability of the input source. The input source capability is qualified by the internal active detection circuit.

Once the input source passes all the conditions above, the status register BUS_GD bit will go high. An INT is asserted to the host.

Input Source Type Detection

After the BUS_GD bit goes high and REGN LDO is powered, the charger device will run input source type detection when a DC source plugs in.

The SY6974 can set input current limit through PSEL pin.

The host can over-write IINLIM register to change the input current limit if needed.

After the input source type detection is done, an INT pulse is asserted to the host.

PSEL Pin Sets Input Current Limit

The PSEL pin directly will take the USB PHY device output to decide whether the input is USB host or charging port. When the device is in default mode, IINDPM will be updated by PSEL value in real time. When the device is in host mode, IINDPM will be set by host, and can force an updating by reading PSEL value if set FORCE_INDET bit.

Input detection	PSEL	Input Current Limit	BUS_STAT
USB SDP(USB500)	High	500mA	001
Adapter	Low	2.4A	011

Force Input Current Limit Detection

The host can force the charger to run input current limit detection by setting FORCE_INDET bit in host mode (FORCE_INDET bit returns to 0 after a force detection finished).

Input Voltage Limit Setting

The device supports wide range of input voltage limit (3.9V-5.4V) source and provides two methods to set input voltage limit (VINDPM) threshold to facilitate autonomous detection.

1. VINDPM based on VINDPM[3:0] register bits. (Register VDPM_BAT_TRACK=00)
2. VINDPM based on the higher of the VINDPM register bits and VBAT + VDPM_BAT_TRACK offset. (Register VDPM_BAT_TRACK not 00)

Converter Power up

After the input current and voltage are set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET will turn off. Otherwise, BATFET will stay on to charge the battery.

The SY6974 will provide soft-start when ramps up the system rail. When the system rail is below 2.2V, the input current limit will be 200mA.

As a battery charger, the SY6974 deploys a 1.5MHz Buck regulator. Internal compensation network allows minimizing the peripheral circuit design.

In order to improve light-load efficiency, the device switches to PFM control at light load.

Boost Mode Operation from Battery

The SY6974 supports Boost converter operation to deliver power from the battery to other portable devices.

The Boost mode output current rating meets the USB On-The-Go 500mA output requirement. The maximum output current on BUS is 1.2A.

Any fault during Boost operation, including BUS over voltage, or over current, or battery too low (V_{BAT}<V_{OTG_BAT}), sets the BOOST_FAULT register to 1 and an INT is asserted.

During Boost mode, the status register BUS_STAT is set to 111, the BUS output is 5.15V by default and the output current limit can reach up to 1.2A, selected via I^2C (BOOST_LIM bits).

Power Path Management

The SY6974 accommodates a wide range of input sources from USB, wall adapter, or car battery. The device provides automatic power path selection to supply the system (SYS) from input source (BUS), battery (BAT), or both.

Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by SYS_MIN bits. Even with a fully depleted battery the system is regulated above the minimum system voltage (default 3.5V)

The status register VSYS_STAT bit goes high when the system is in minimum system voltage regulation.

Dynamic Power Management

The SY6974 can management the input power limit very well. It has input VINDPM and IINDPM function to protect the input source from over-loading.

When input source is over-loaded, either the current exceeds the input current limit (IINLIM) or the voltage will fall below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero but the input source is still overloaded, the system voltage will start to drop. Once the system voltage falls below the battery voltage, the device will automatically enter the supplement mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

During DPM mode the status register VDPM_STAT or IDPM_STAT will go high.

Battery Charging Management

The SY6974 charges 1-cell Li-ion battery with up to 3.0A charge current for high capacity tablet battery. The 17mΩ BATFET improves charging efficiency and minimizes the voltage drop during discharging.

Autonomous Charging Cycle

With battery charging enabled at POR (CHG_CONFIG bit =1 and /CE pin is low), the SY6974 can complete a charging cycle without host involvement. The device default charging parameters are listed below.

Charging Parameter	Default Setting
Charging Voltage	4.208V
Charging Current	2.048A
Pre-charge Current	180mA
Termination Current	180mA
Temperature Profile	JEITA
Safety Timer	10 hours

The charger device will automatically terminate the charging cycle when in constant voltage charge and the charging current is below termination threshold. When a full battery voltage is discharged below recharge threshold (REG04[0]), the SY6974 will automatically start another charging cycle.

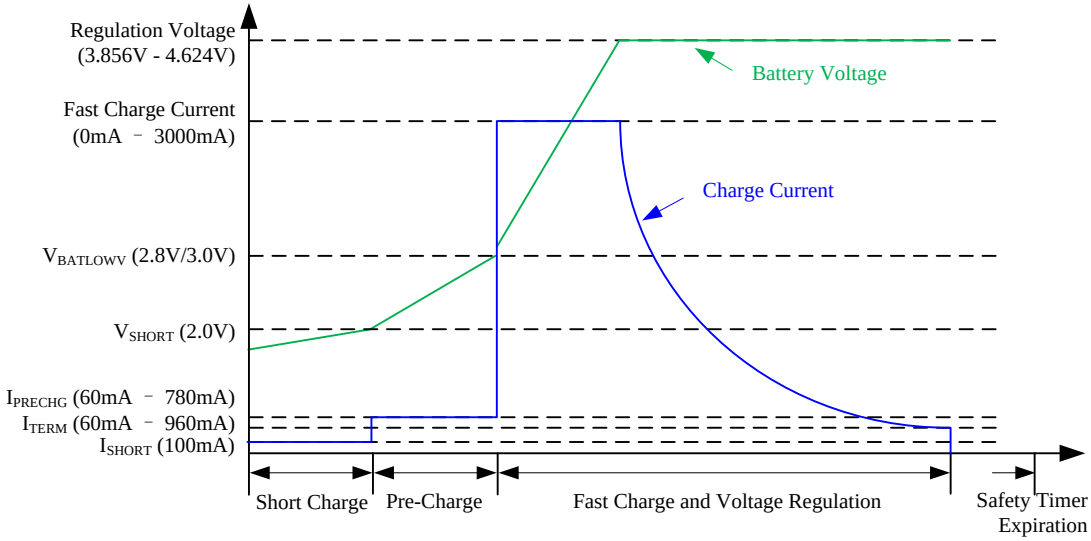
The STAT output indicates the charging status of charging (LOW), charging completion or charge disable (HIGH) or charging fault (Blinking). The STAT output can be disabled by setting STAT_DIS bit. The status register CHRG_STAT indicates the different charging phases: 00-charging disable, 01-precharge, 10-fast charge (constant current) and constant voltage mode, 11-charging done. Once a charging cycle is complete, an INT will be asserted to notify the host.

The host can always control the charging operation and optimize the charging parameters by writing to the registers through I^2C.

Battery Charging Profile

The device charges the battery in five phases: battery short, preconditioning, constant current and constant voltage and top-off charging (optional). At the beginning of a charging cycle, the device checks the battery voltage and applies current.

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.



Charging Termination

The SY6974 will terminate a charge cycle when in constant voltage charge, and the current is below termination current. After the charging cycle is complete, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn back on to engage supplement mode.

When termination occurs, the CHRG_STAT will be 11, and an INT is asserted to the host. Termination can be disabled by writing 0 to EN_TERM.

A programmable top-off timer can be applied after termination is detected. The host can read CHRG_STAT and TOPOFF_ACTIVE to find out the termination status.

The top-off timer settings are read in once termination is detected by the charger. Programming a top-off timer value after termination will have no effect unless a recharge cycle is initiated. An INT will be asserted to the host when entering top-off timer segment (due to termination) as well as when top-off timer expires.

Charging Safety Timer

The SY6974 has safety timer to prevent extended charging cycle due to abnormal battery conditions.

The device will keep charging the battery until the fast charging safety timer expired. The duration of safety timer can be set by the CHG_TIMER bits (default 10 hours). Once the safety timer is expired, the fault register CHRG_FAULT bits will be set to 11 and an INT will be asserted to the host. The safety timer feature can be disabled by setting EN_TIMER bit.

The safety timer will be 2 hours when the battery is below $V_{BATLOWV}$ threshold.

During input voltage/current regulation or thermal regulation or JEITA cool, the safety timer counts at half clock rate. For example, if the charger is in input current regulation (IINDPM) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will expire in 10 hours. This feature can be disabled by writing 0 to REG07[6] (bit TMR2X_EN).

Host Mode and Default Mode

The SY6974 can operate with or without host. In default mode, the SY6974 can be used as an autonomous charger with no host or with host in sleep.

When the charger is in default mode, WATCHDOG_FAULT bit is high. When the charger is in host mode, WATCHDOG_FAULT is low.

After power-on-reset, the device starts in default mode. The registers are in the default settings.

Any host writing command to I^2C transitions the device from default mode to host mode. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires or disable watchdog timer by setting WATCHDOG bit to 0.

When the watchdog timer is expired, the device gets back to the default mode.

Status Outputs (/PG STAT and /INT)

Power Good Indicator (/PG)

In the SY6974, /PG goes LOW to indicate a good input source.

Charging Status Indicator (STAT)

The SY6974 indicates charging state on the open drain STAT pin. The STAT pin can drive LED as the application diagram shows.

STAT Pin State	
CHARGING STATE	STAT
Charging in progress (including recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH
Charge suspend (Input over-voltage, NTC fault, timer fault, input or system over- voltage) Boost Mode suspend (due to NTC Fault)	blinking at 1Hz

Interrupt to Host (INT)

In some applications, the host does not always monitor the charger operation. The INT notifies the system on the device operation.

When a fault occurs, the charger device will send out INT and latches the fault state in REG09 until the host reads the fault register. Before the host reads REG09 and all the faults (not including watchdog timer fault) are cleared, the charger device would not send any INT upon new faults.

In order to read the current fault status, the host has to read REG09 two times consecutively. The 1st reads fault register status from the last INT and the 2nd reads the current fault register status. The only exception is NTC_FAULT which always reports the actual condition on the NTC pin.

BATFET (Q4) Control

BATFET Disable Mode (Shipping mode)

To extend battery life and minimize power when system is powered off during system idle, shipping, or storage, the device can turn off BATFET so that the system voltage is zero to minimize the battery leakage current.

When the host set BATFET_DIS bit, the charger can turn off BATFET immediately or delay by t_{SM_DLY} as configured by BATFET_DLY bit.

BATFET Enable Mode (Exit Shipping mode)

When the BATFET is disabled (**in shipping mode**) and indicated by setting BATFET_DIS, plugging in adapter or a logic transition from high to low on /QON pin with t_{QON_LOW} time can enable BATFET to exit shipping mode.

BATFET System Reset

The BATFET functions as a load switch between battery and system when input source is not plugged-in and BATFET_DIS=0. By changing the state of BATFET from OFF to ON, system connects to SYS can be effectively have a power-on-reset.

This function can be disabled by setting BATFET_RST_EN bit to 0.

Protections

Thermal Regulation and Thermal Shutdown

Buck Mode

The SY6974 monitors the internal junction temperature T_J to avoid overheat the chip and limits the IC surface temperature. When the internal junction temperature exceeds the preset limit (TREG bits), the device lowers down the charge current. The thermal regulation range from 90℃ to 110℃ allows the user to optimize the system thermal performance.

During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register THERM_STAT goes high.

Additionally, the device has thermal shutdown to turn off the converter and BATFET. The fault register

CHRG_FAULT is 10 and an INT is asserted to the host. The BATFET and converter are enabled to recover when IC temperature is below T_{TSD}-T_{TSD_HYS}.

Boost Mode

The device monitors the internal junction temperature to provide thermal shutdown during Boost mode. When IC junction temperature exceeds T_{TSD}, the Boost mode is disabled by setting OTG_CONFIG low.

Voltage and Current Monitoring in Buck Mode

SY6974 closely monitors the input and system voltage, as well as HSFET and LSFET current for safe Buck mode operation.

Input over-Voltage (ACOV)

If BUS voltage exceeds V_{ACOV}, the device stops switching immediately. During input over voltage (ACOV), the fault register CHRG_FAULT will be set to 01. An INT is asserted to the host.

System over-Voltage Protection (SYSOVP)

The charger device monitors the voltage at SYS. When system over-voltage is detected, the converter is stopped to protect components connected to SYS from high voltage damage.

Voltage and Current Monitoring in Boost Mode

SY6974 closely monitors the BUS voltage, as well as HSFET and LSFET current to ensure safe Boost mode operation.

Over Current Protection

The charge device closely monitors the RBFET(Q1), HSFET(Q2) and LSFET(Q3) current to ensure safe Boost operation.

During over-current condition when output current exceeds (BOOST_LIM) the device will retry 7 times in hiccup mode for protection. If the over current condition is removed within 7 times retry, the Boost converter will recover the OTG output. If over-current condition continues to exist after 7 times retry, Boost will be disabled with OTG_CONFIG bit cleared, in addition, the BOOST_FAULT bit is set and INT pulse is generated.

Over Voltage Protection

Once the BUS voltage exceeds V_{OTG_OVP}, SY6974 stops switching immediately, and clears OTG_CONFIG bit and exits Boost mode. And the fault register BOOST_FAULT is set high to indicate fault in Boost operation. An INT is asserted to the host.

Battery Protection

Battery Over-Voltage Protection (BATOVP)

The battery over-voltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charge. The fault register BAT_FAULT goes high and an INT is asserted to the host.

Battery over Discharge Protection

When battery voltage is discharged below V_{BAT_DPL}, the BATFET is turned off to protect battery from over discharge. To recover from over-discharge, an input source is required at BUS. When an input source is plugged in, the BATFET turns on again.

If the battery voltage falls below V_{SHORT}, the charge current is reduced to short charge or pre-charge current for battery safety.

System over Current Protection

If the system is shorted or BATFET OCP occurs, the BATFET is latched off. Section “BATFET Enable Mode” can reset the latch off condition and turn on BATFET.

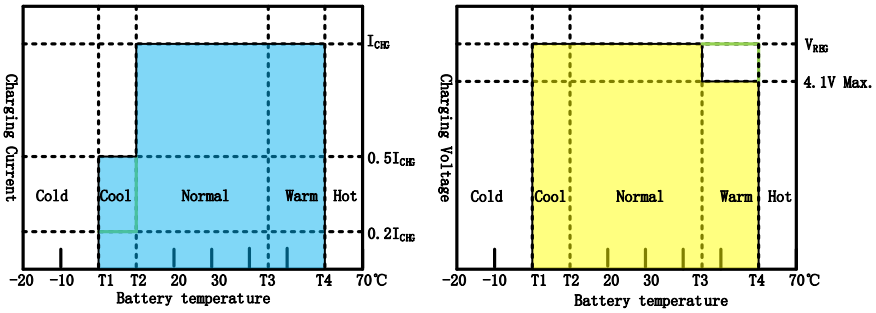
Thermistor Temperature Window

SY6974 continuously monitors battery temperature by measuring the voltage between the NTC pin and ground, typically determined by a negative temperature coefficient thermistor and an external voltage divider.

Charging JEITA Guideline Compliance

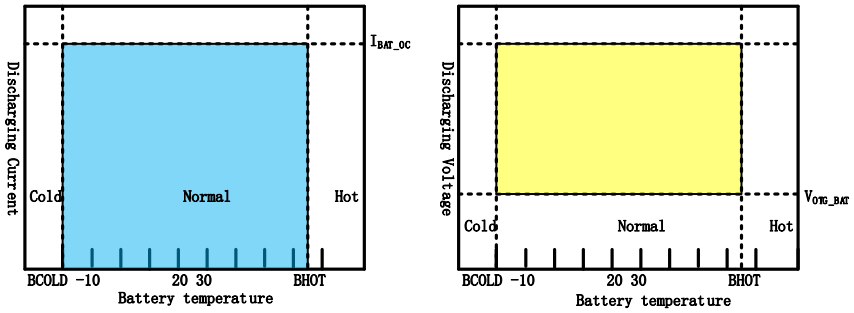
JEITA recommends suspending the battery charging process when NTC pin voltage is out of the V_{T1} to V_{T4} range, and recovering charging process once the NTC voltage is within the range. JEITA also recommends that the charge current to be reduced to at least half of the charge current or lower at cool temperature (T1–T2), and the charge voltage to be reduced less than nominal charge voltage at warm temperature (T3–T4).

SY6974 provides flexibility voltage/current settings beyond the JEITA requirement. The voltage setting at warm temperature (T3–T4) can be V_{REG} or 4.1V max. (REG07[4]). The current setting at cool temperature (T1–T2) can be further reduced to 50% or 20% of fast charge current (REG05[0]).



Discharging Cold/Hot Temperature Window

The device will terminate the battery discharging process when NTC pin voltage is out of the V_{BCOLD} to V_{BHOT} range. To allow the discharge, the battery temperature must be within this range.



When the NTC fault occurs, the fault register NTC_FAULT will indicate the actual condition on NTC pin and an INT will be asserted to the host. The STAT pin will indicate the fault when discharging is suspended.

Serial Interface

The SY6974 uses I²C compatible interface for flexible charging parameter programming and instantaneous device status reporting. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6BH, receiving control inputs from the master device like micro controller or a digital signal processor. The I²C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits).

Both SDA and SCL are bi-directional lines, connecting to the positive supply voltage via a current source or pull- up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

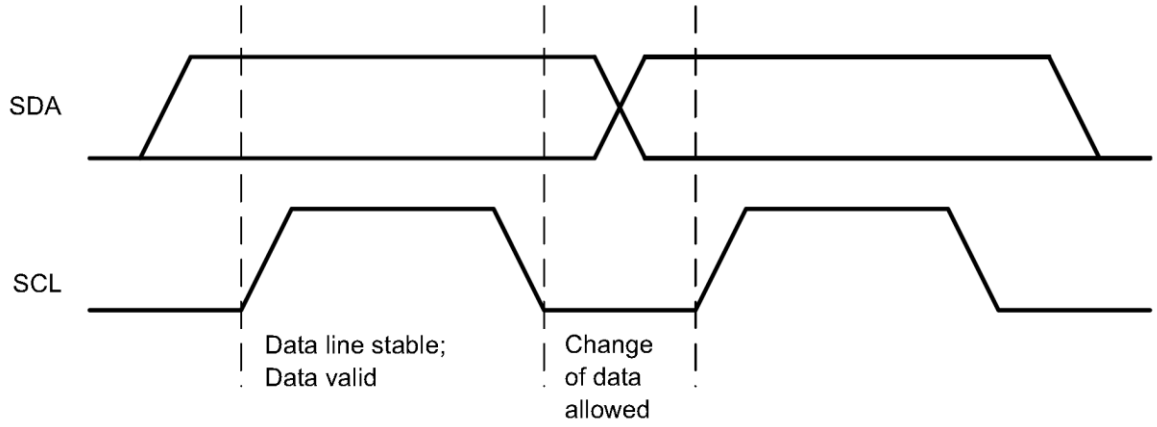


Figure 3. Bit Transfer on the I²C Bus

START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCl is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

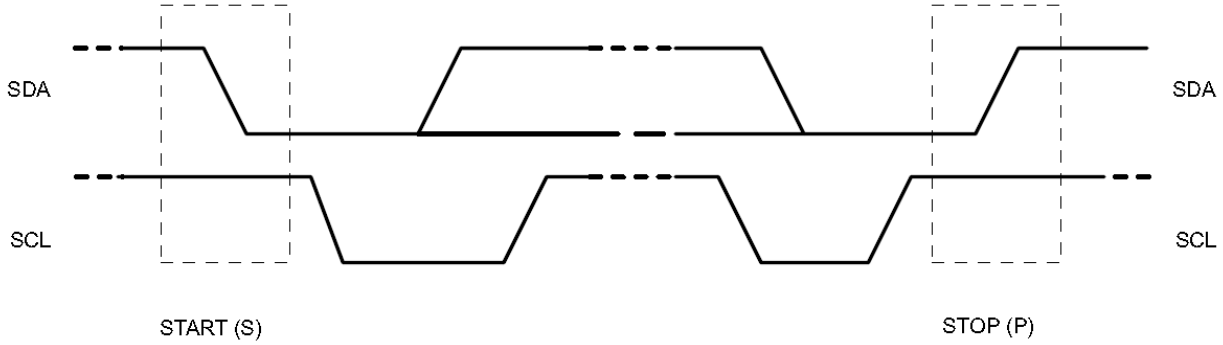


Figure 4. START and STOP Conditions

Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

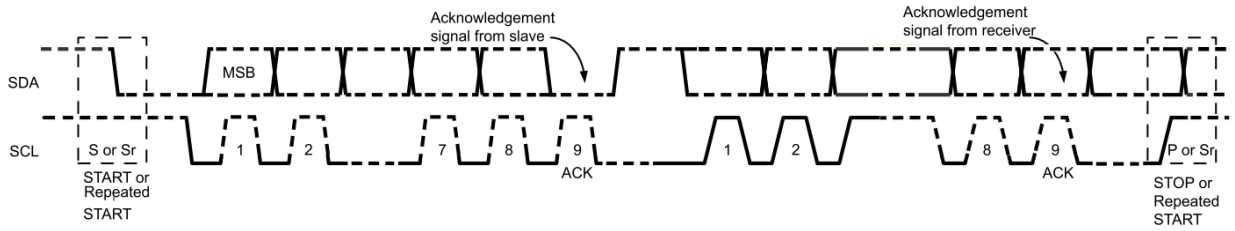


Figure 5. Data Transfer on the I²C Bus

Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the 9th acknowledge clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

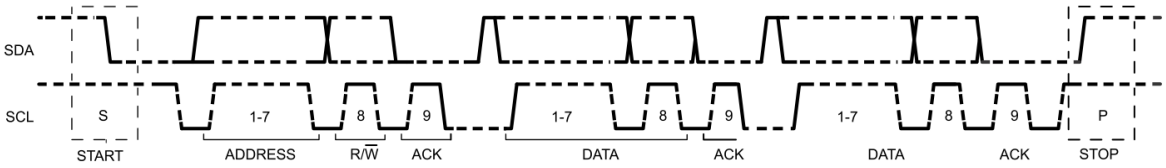


Figure 6. Complete Data Transfer

Single Read and Write

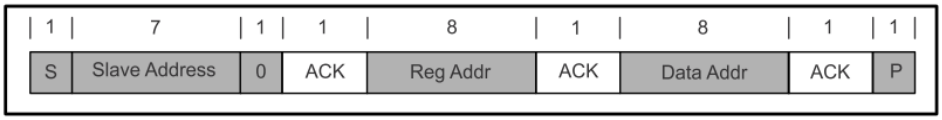


Figure 7. Single Write

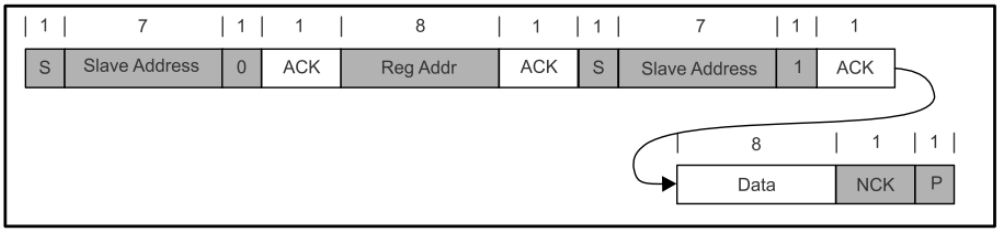


Figure 8. Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG08.

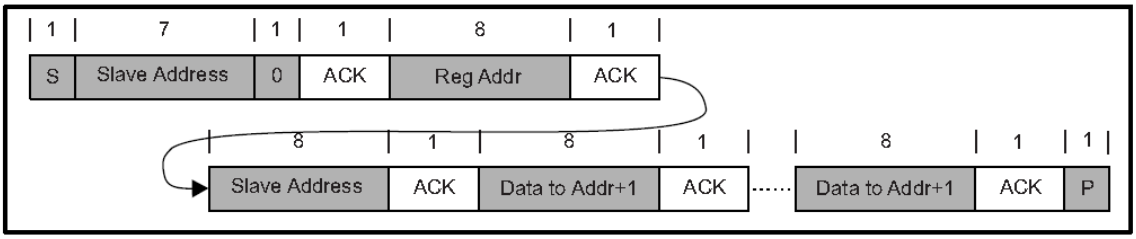


Figure 9. Multi-Write

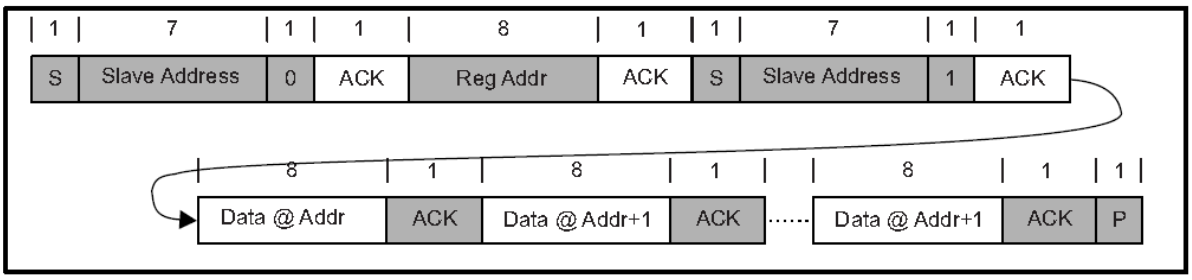


Figure 10. Multi-Read

The fault register REG09 locks the previous fault and only clears it after the register is read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REG09 reports the fault when it is read the first time, but returns to normal when it is read the second time. To verify real time fault, the fault register REG09 should be read twice to get the real condition. In addition, the fault register REG09 does not support multi-read or multi-write.

Applications Information

The following battery charger design refers to the "Application Schematic". This section describes how to select the external components including the inductor, the input and output capacitors.

Inductor Selection

Higher switching frequency allows the using of the smaller inductor and the capacitor values. The inductor saturation current should be higher than the load current (I_{LOAD}) plus half of the ripple current (I_{Ripple}):

$$I_{SAT} \geq I_{LOAD} + \frac{1}{2} \times I_{Ripple}$$

The inductor ripple current depends on the input voltage (V_{IN}), the duty cycle ($D = V_{OUT}/V_{IN}$), the switching frequency (F_{SW}) and the inductance (L):

$$I_{Ripple} = \frac{V_{IN} \times D \times (1-D)}{F_{SW} \times L}$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. Usually the inductor ripple is designed in the range of (20-40%) maximum charging current as a trade-off between the inductor size and efficiency for a practical design.

Output Capacitor Selection

The output capacitor in parallel with the battery is used for absorbing the high frequency switching ripple current and smoothing the output voltage. The RMS value of the output ripple current I_{RMS} is calculated as follow:

$$I_{RMS} = \frac{V_{IN} \times D \times (1-D)}{\sqrt{12} L \times F_{SW}}$$

Where the duty cycle D is the ratio of the output voltage (battery voltage) over the input voltage for CCM mode which is the typical operation for the battery charger. During the battery charge period, the battery voltage varies from its initial battery voltage to the rated voltage. A typical 10μF ceramic capacitor is a good choice to absorb this current and also has a very small size.

Input Capacitor Selection

The input capacitor absorbs input ripple current from the Buck converter, which is given by the below equation:

$$I_{RMS} = \frac{I_{LOAD} \times \sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V}$$

This RMS ripple current must be smaller than the rated RMS current in the capacitor datasheet. At the same time, the input capacitor is also as the output capacitor when Boost works. At this condition, the input capacitor can be calculated as below:

$$C_{IN} = \frac{I_{BUS} \times (V_{BUS} - V_{BAT})}{F_{SW} \times V_{BUS} \times V_{RIPPLE}}$$

Usually V_{RIPPLE} is designed less than 0.5% of the Boost output voltage. A typical 10μF ceramic capacitor is a good choice to absorb this current and also has a very small size. For best performance, V_{BUS} should be decoupled to PGND with 1μF capacitance. The remaining input capacitor should be place on PMID.

Layout Design

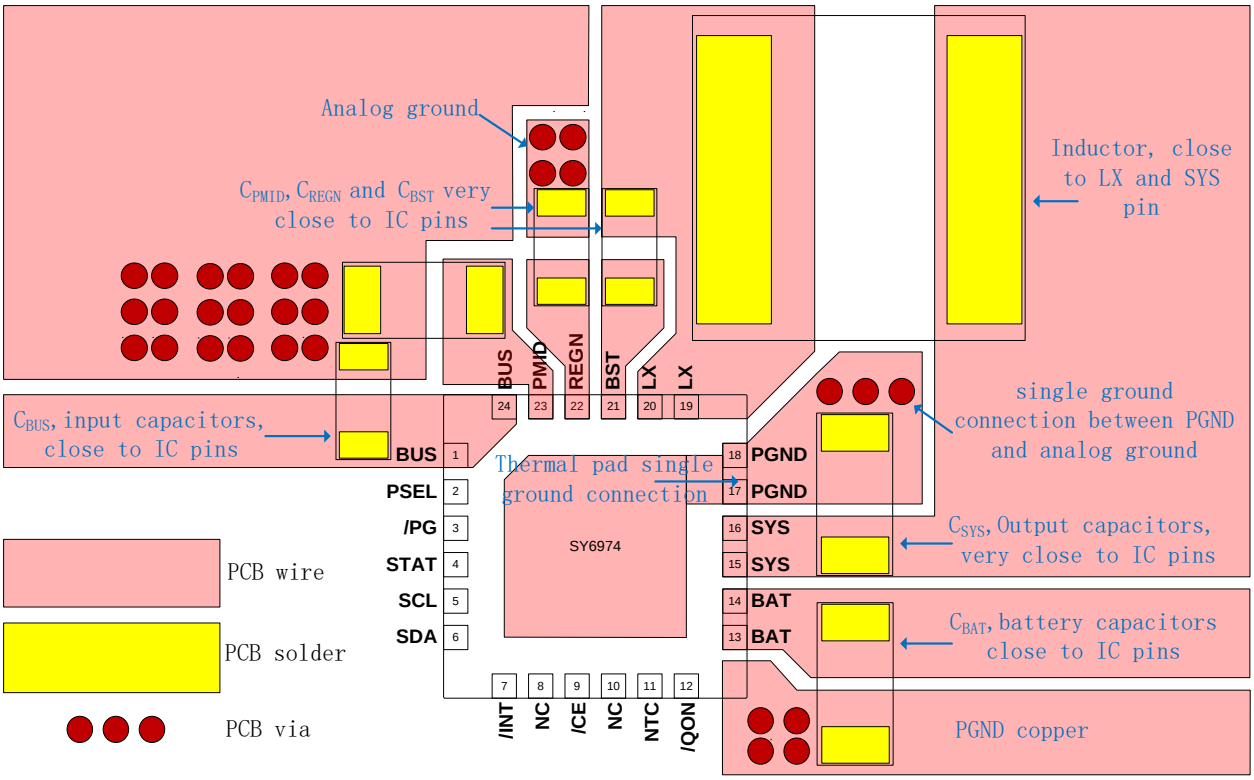
The layout design of SY6974 regulator is relatively simple. For the best efficiency and to minimize noise problems, we should place the following components close to the IC: C_{PMID}, C_{REGN}, C_{BST}, C_{SYS} and C_{BAT}.

1) It is desirable to maximize the PCB copper area adjacent to PGND pin to achieve the best thermal and noise performance. If the board space allows, a ground plane is highly desirable.

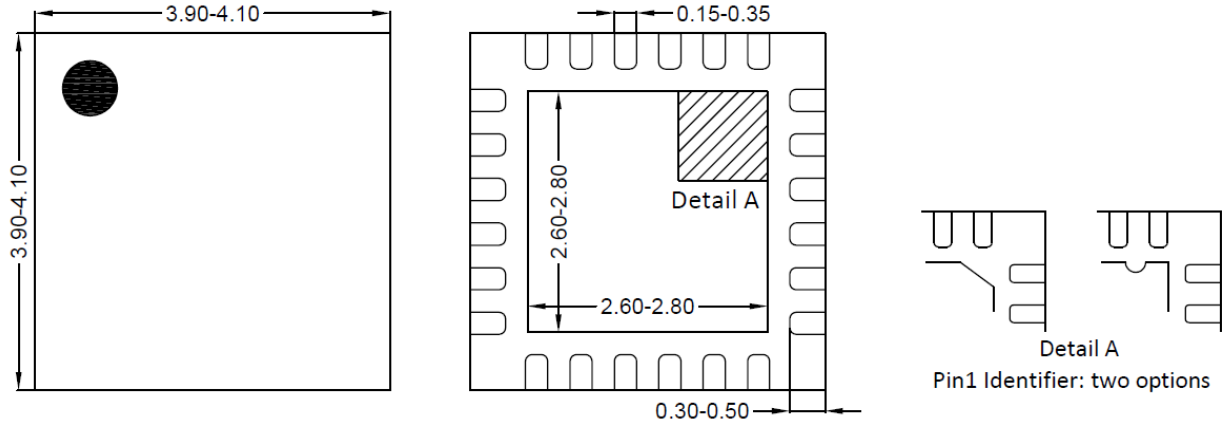
2) C_{PMID}, C_{REGN}, C_{BST}, C_{SYS} and C_{BAT} must be close to the IC.

3) The loop area formed by C_{PMID} and PGND must be minimized. The PCB copper area adjacent to LX pin must be minimized to avoid the potential noise problem.

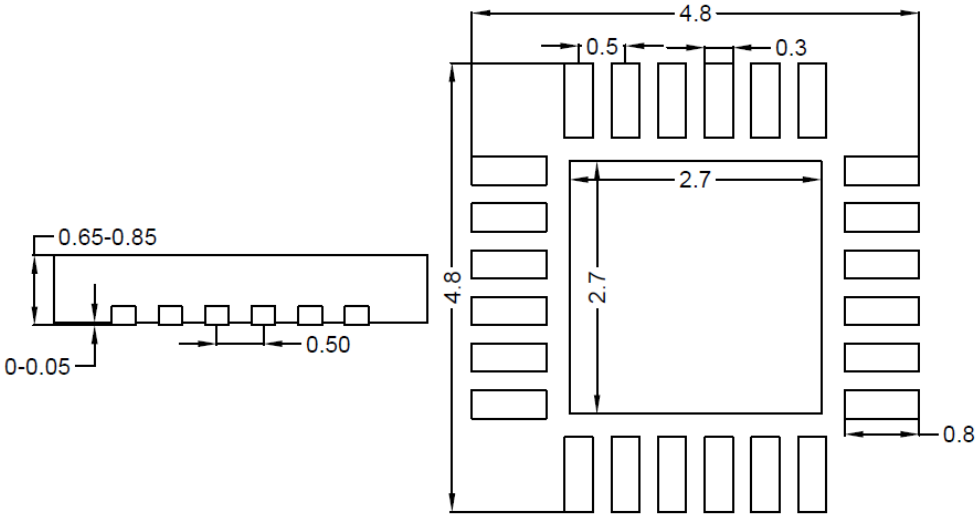
The following picture is the recommended layout design of the inductor, C_{PMID}, C_{REGN}, C_{BST}, C_{SYS} and C_{BAT}.


Analog ground
C_{PMID}, C_{REGN} and C_{BST} very close to IC pins
Inductor, close to LX and SYS pin
C_{BUS}, input capacitors, close to IC pins
single ground connection between PGND and analog ground
Thermal pad single ground connection
C_{SYS}, Output capacitors, very close to IC pins
C_{BAT}, battery capacitors close to IC pins
PGND copper
PCB wire
PCB solder
PCB via
SY6974
BUS 1
PSEL 2
/PG 3
STAT 4
SCL 5
SDA 6
/INT 7
NC 8
/CE 9
NC 10
NTC 11
/QON 12
BAT 13
BAT 14
SYS 15
SYS 16
PGND 17
PGND 18
BUS 24
PMID 23
REGN 22
BST 21
LX 20
LX 19

QFN4x4-24 Package outline & PCB Layout



Top View **Bottom View**

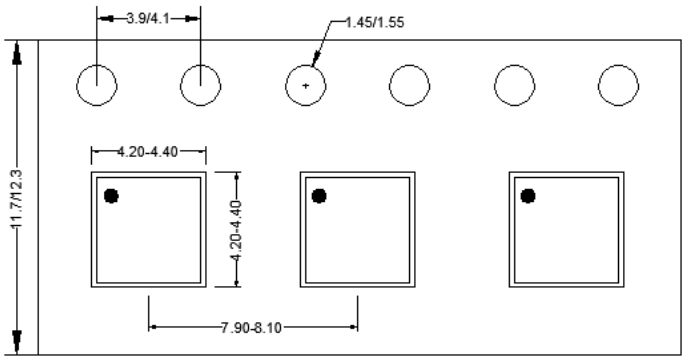


Front View **PCB layout (Recommended)**

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

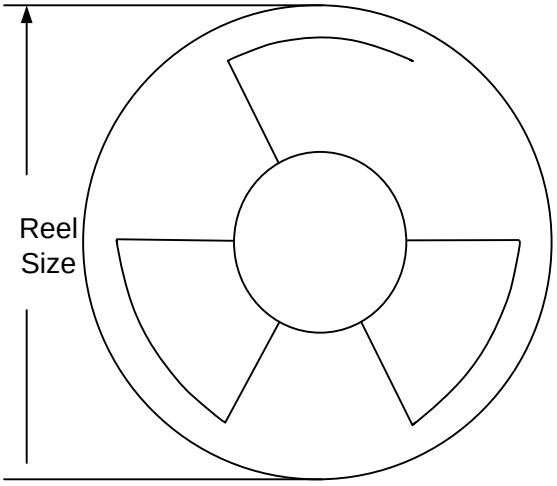
Taping & Reel Specification

1. QFN4x4 taping orientation



Feeding direction

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
QFN4x4	12	8	13"	400	400	5000

3. Others: NA

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